



US009196297B2

(12) **United States Patent**
Yang et al.

(10) **Patent No.:** **US 9,196,297 B2**
(45) **Date of Patent:** **Nov. 24, 2015**

(54) **SYSTEMS AND METHODS FOR ENHANCED SYNC MARK MIS-DETECTION PROTECTION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/896,027**

(22) Filed: **May 16, 2013**

(65) **Prior Publication Data**

US 2014/0268389 A1 Sep. 18, 2014

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Related U.S. Application Data

(60) Provisional application No. 61/785,947, filed on Mar. 14, 2013.

(51) **Int. Cl.**
G11B 20/10 (2006.01)
G11B 20/18 (2006.01)
G06F 11/263 (2006.01)

(52) **U.S. Cl.**
CPC **G11B 20/10305** (2013.01); **G06F 11/263** (2013.01); **G11B 20/10361** (2013.01); **G11B 20/1816** (2013.01); **G11B 20/1037** (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

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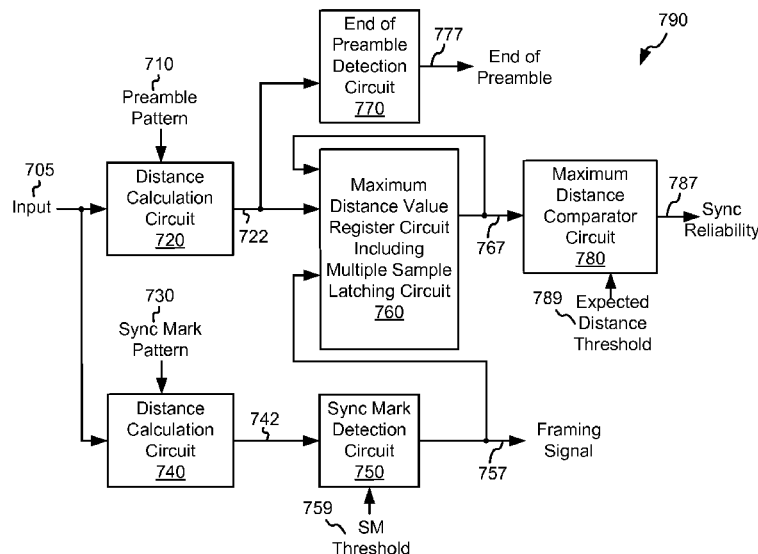
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Primary Examiner — Daniell L Negron

(57) **ABSTRACT**

The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for detecting patterns in a data stream.

20 Claims, 10 Drawing Sheets



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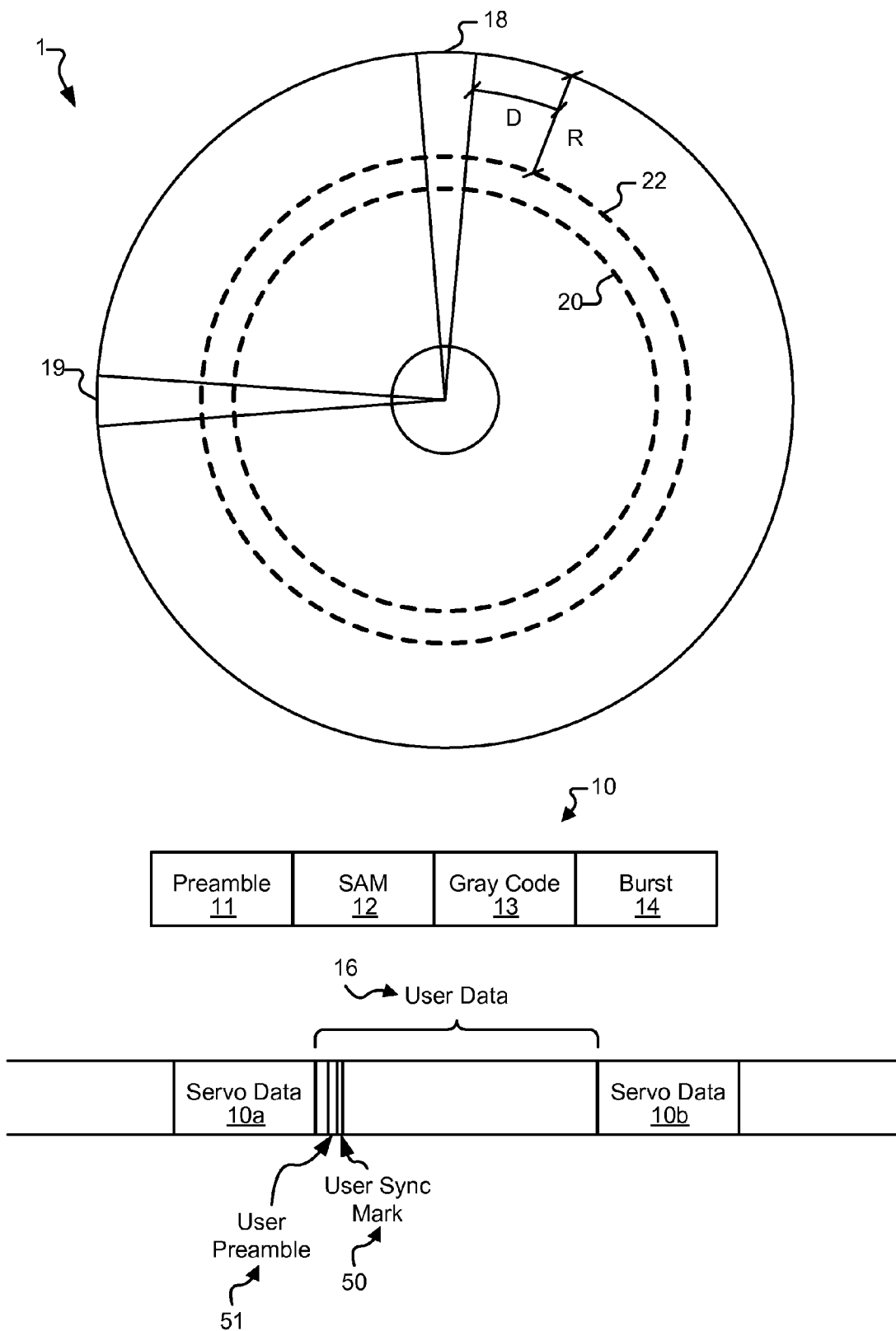


Fig. 1 (Prior Art)

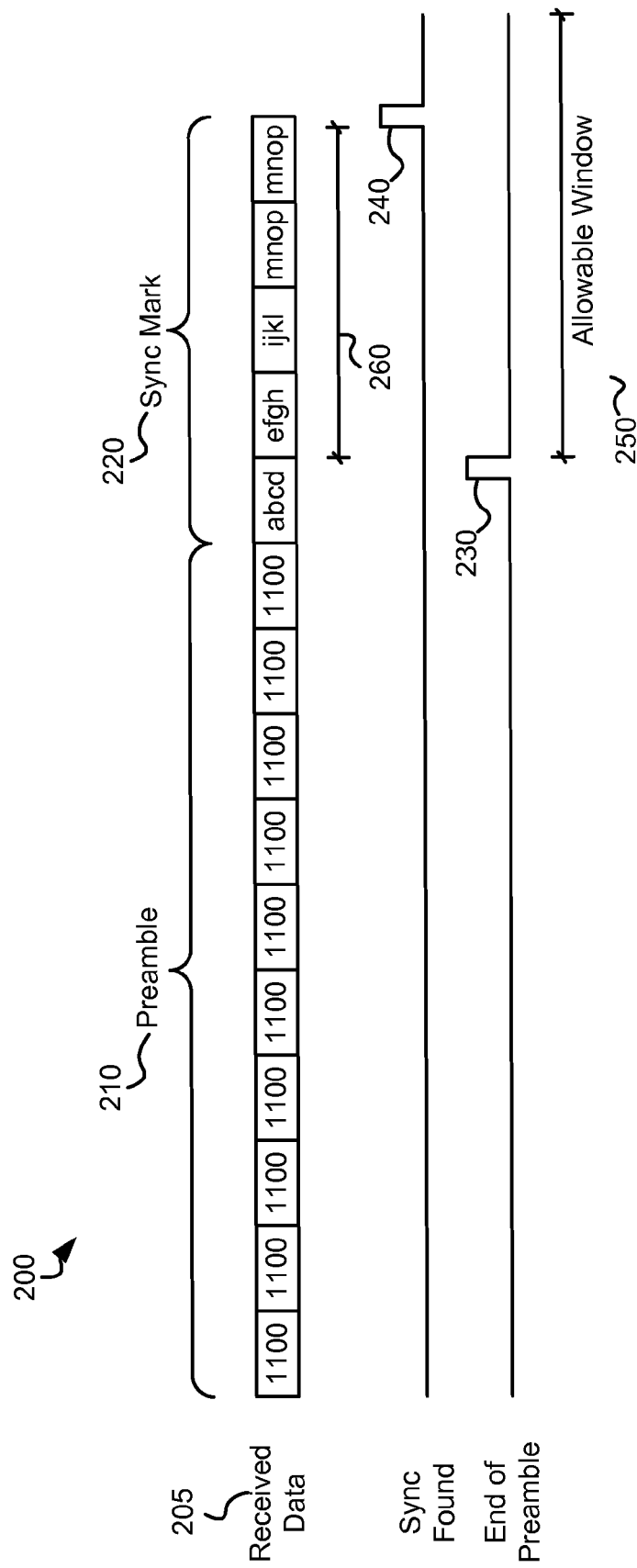


Fig. 2

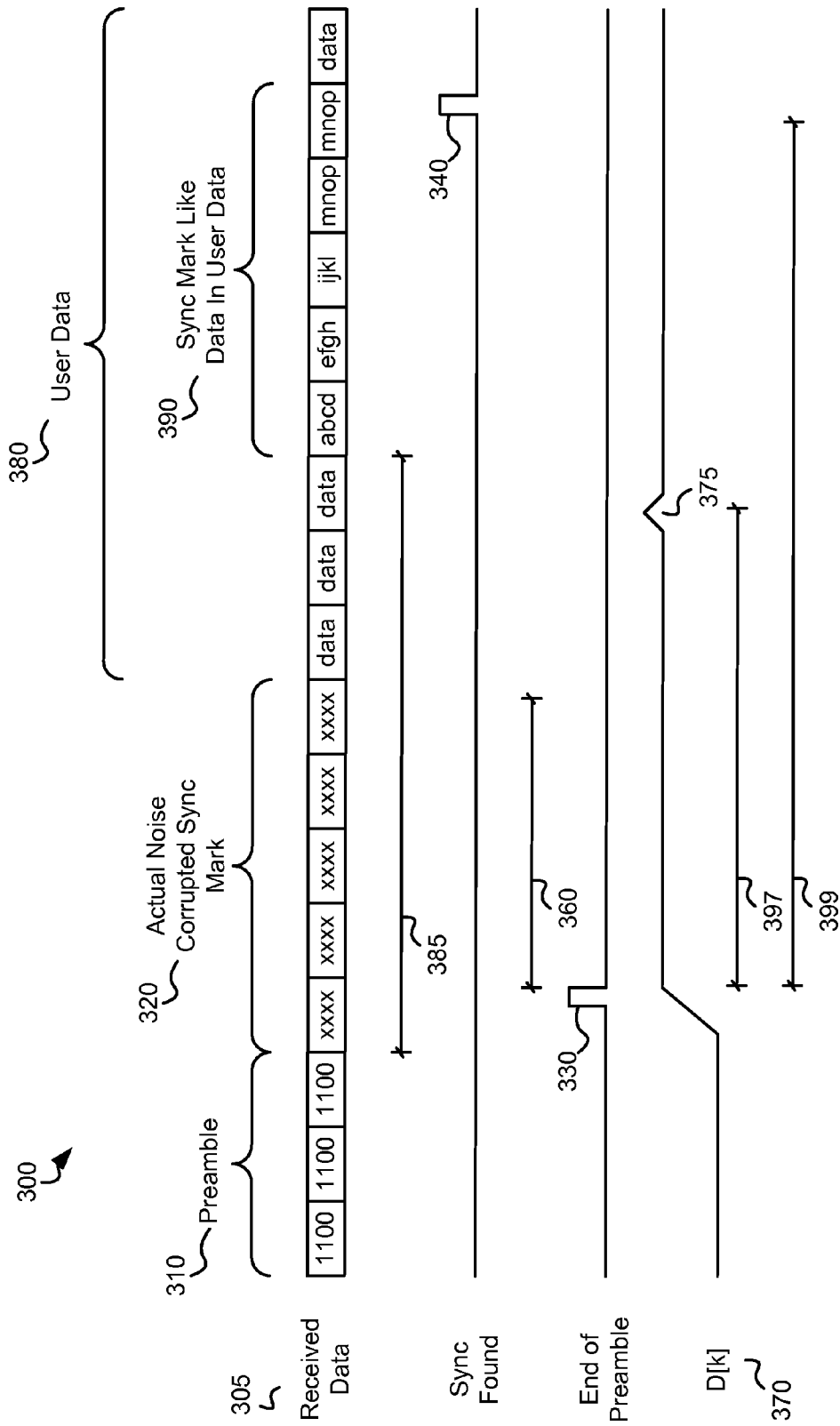


Fig. 3

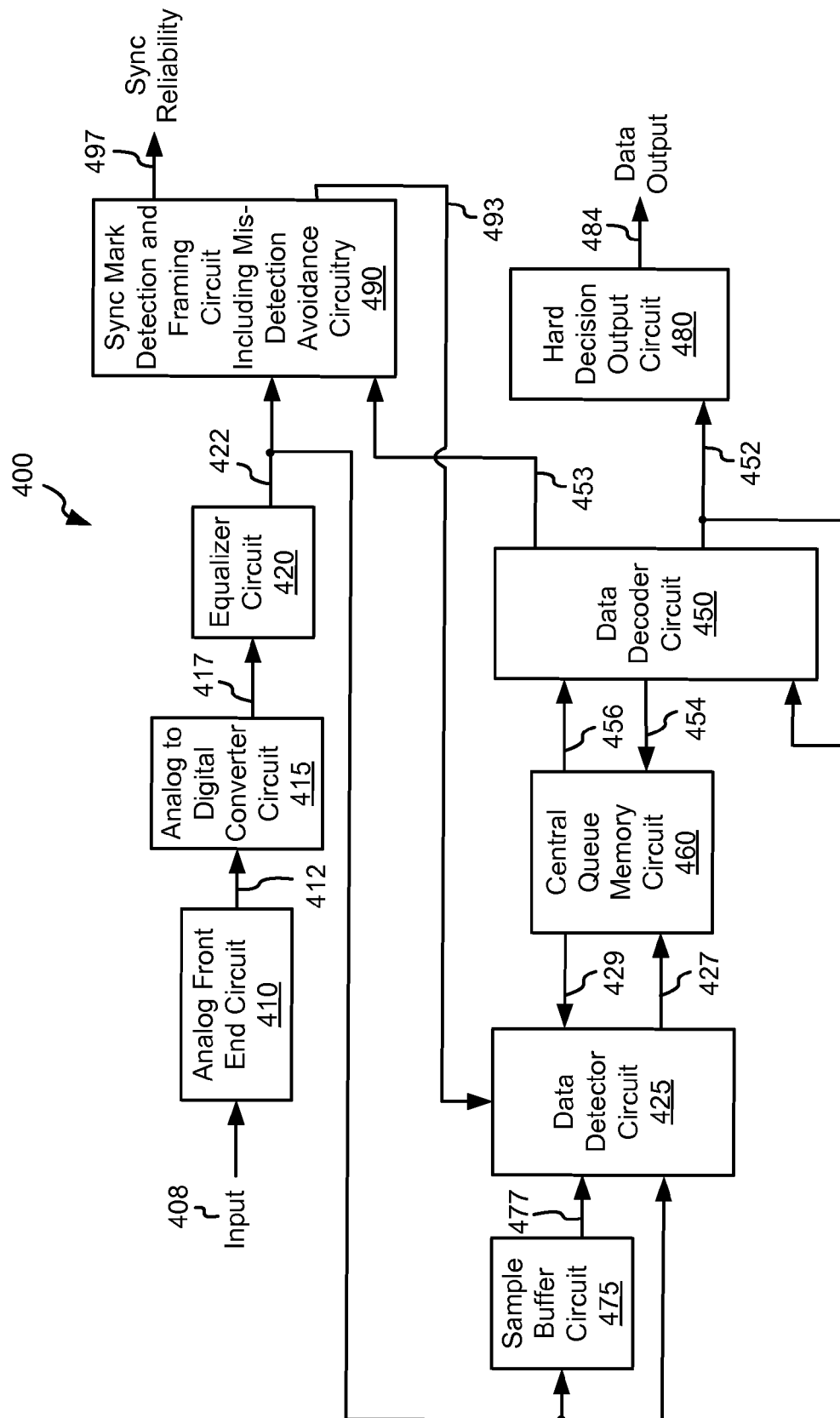


Fig. 4a

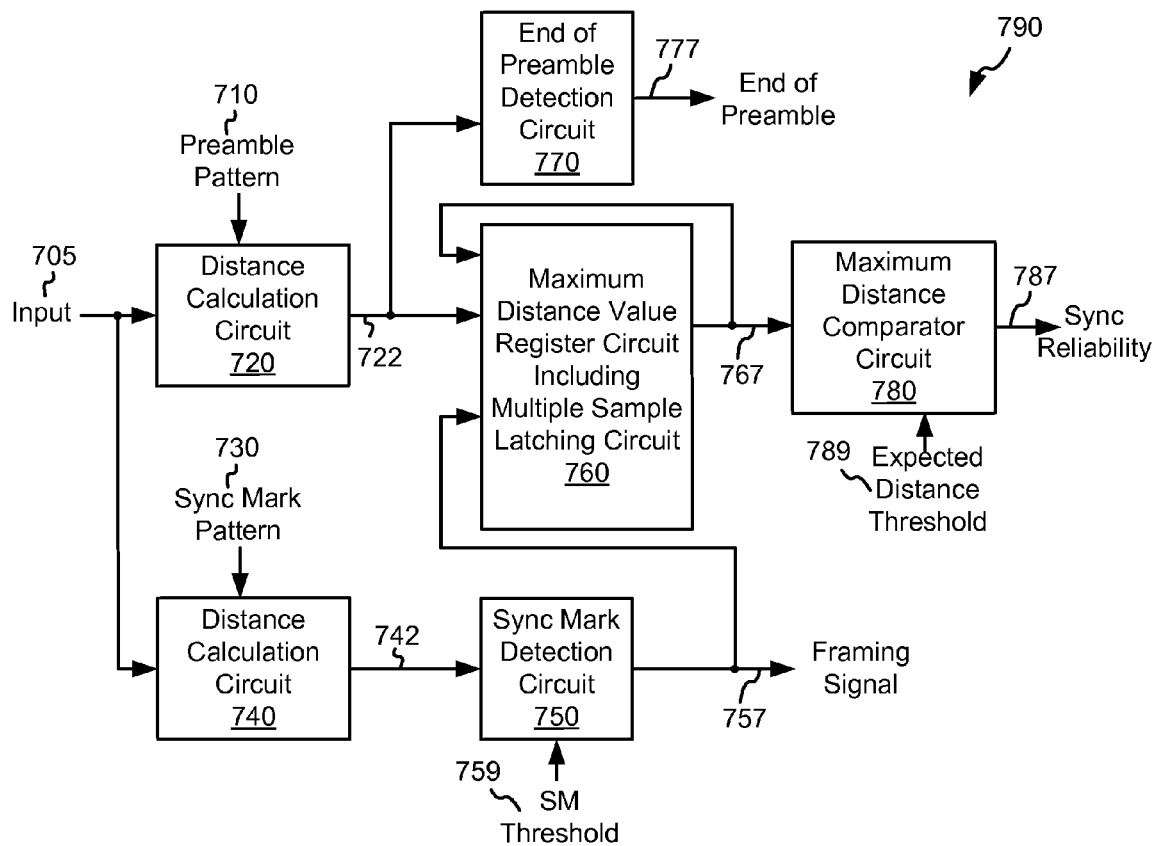


Fig. 4b

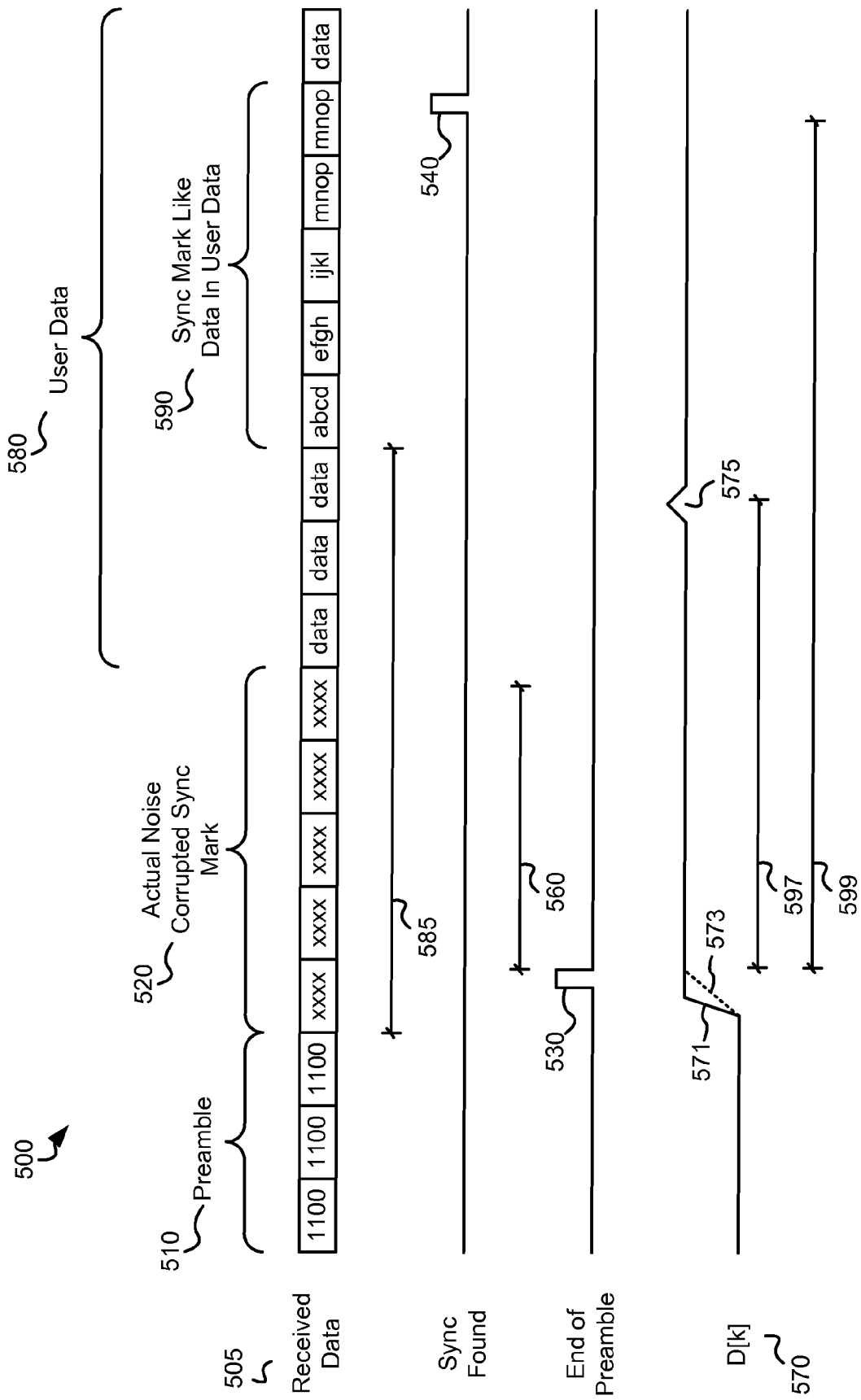


Fig. 5

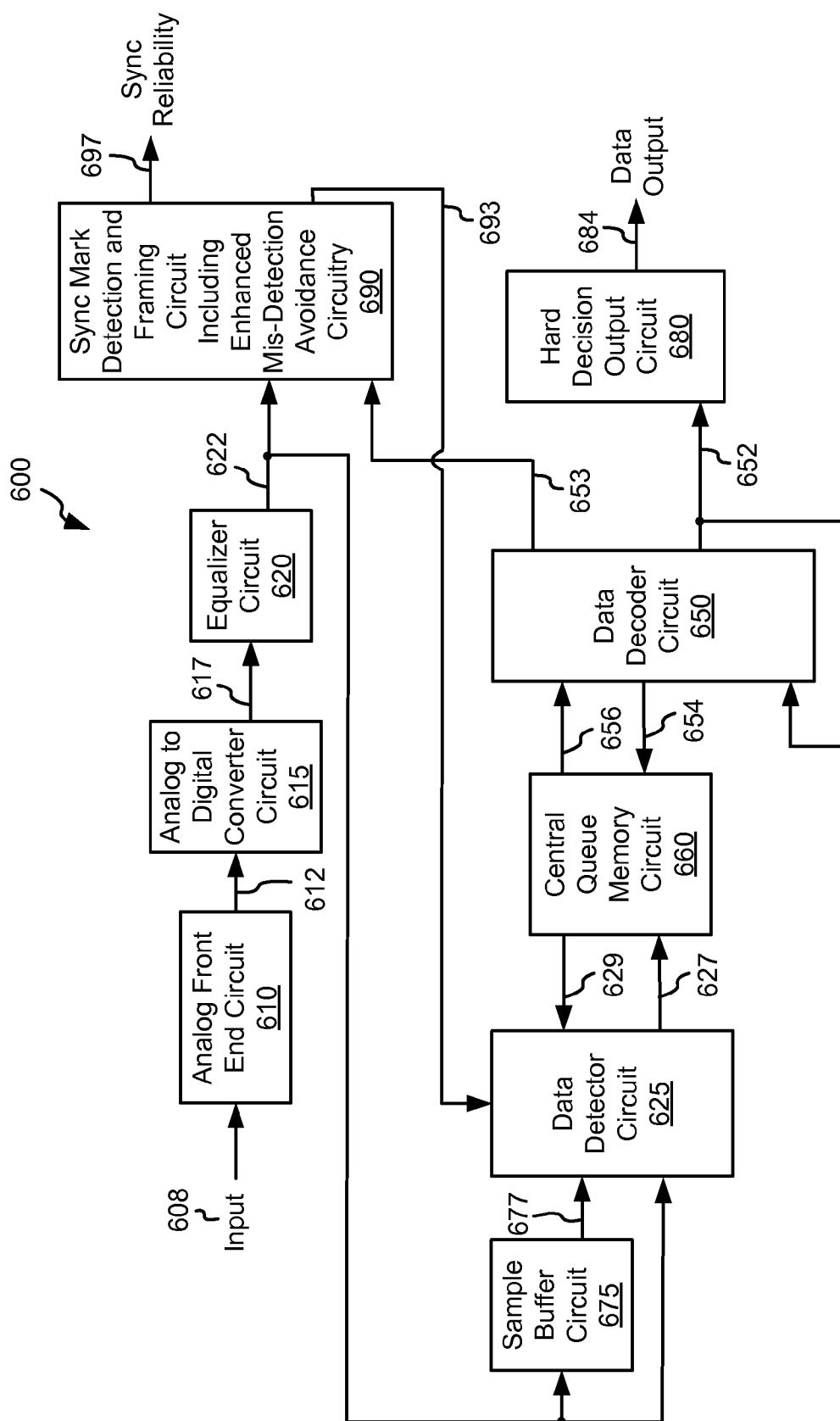


Fig. 6a

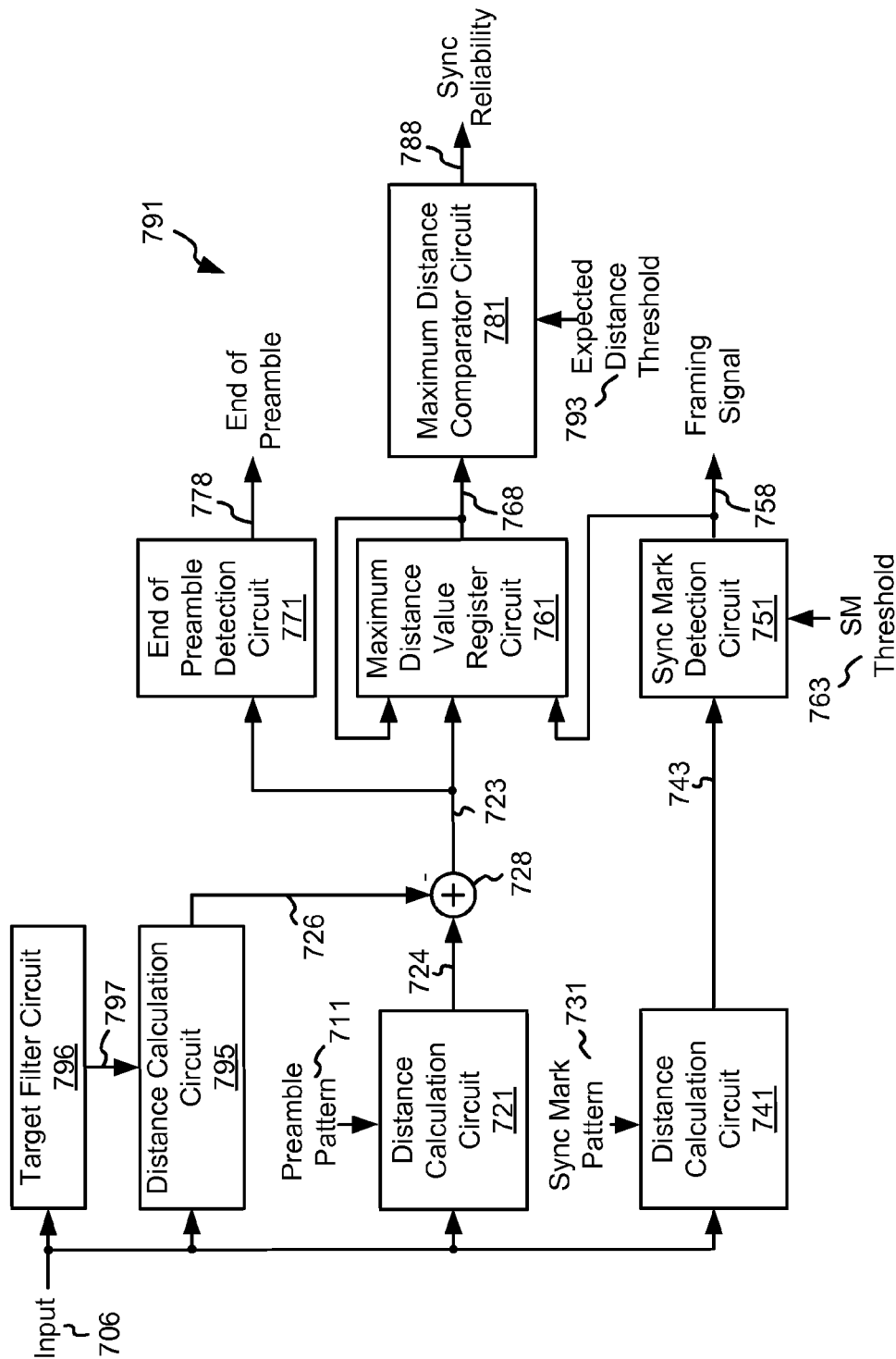


Fig. 6b

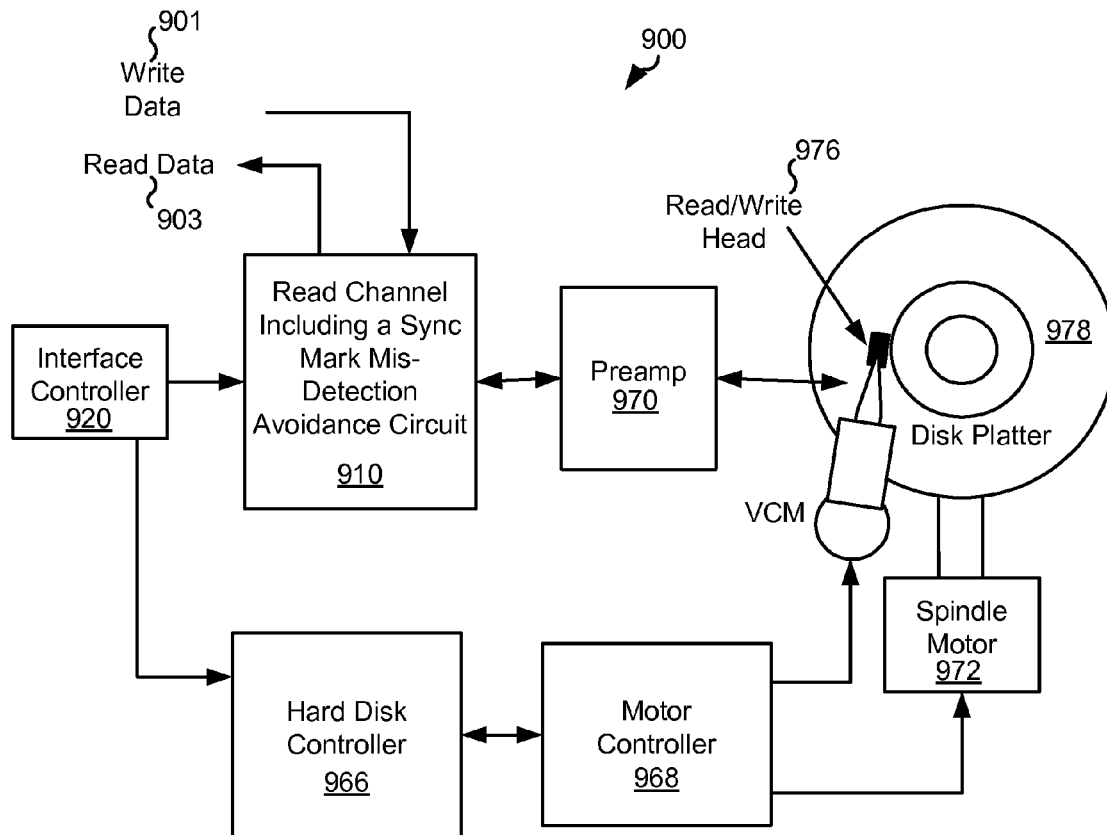


Fig. 7

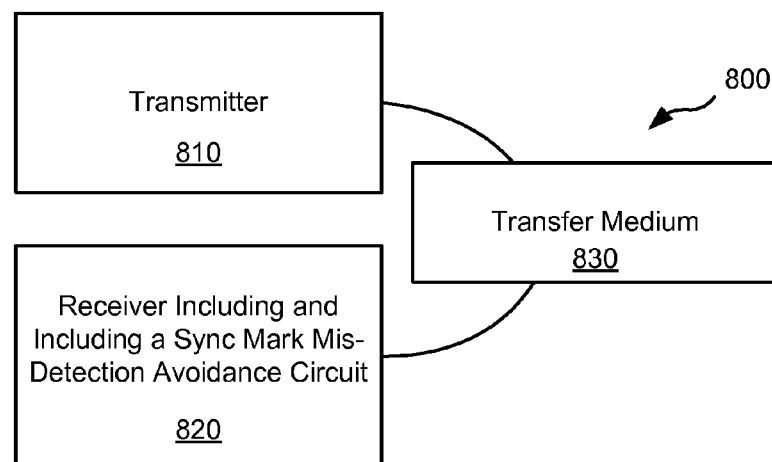


Fig. 8

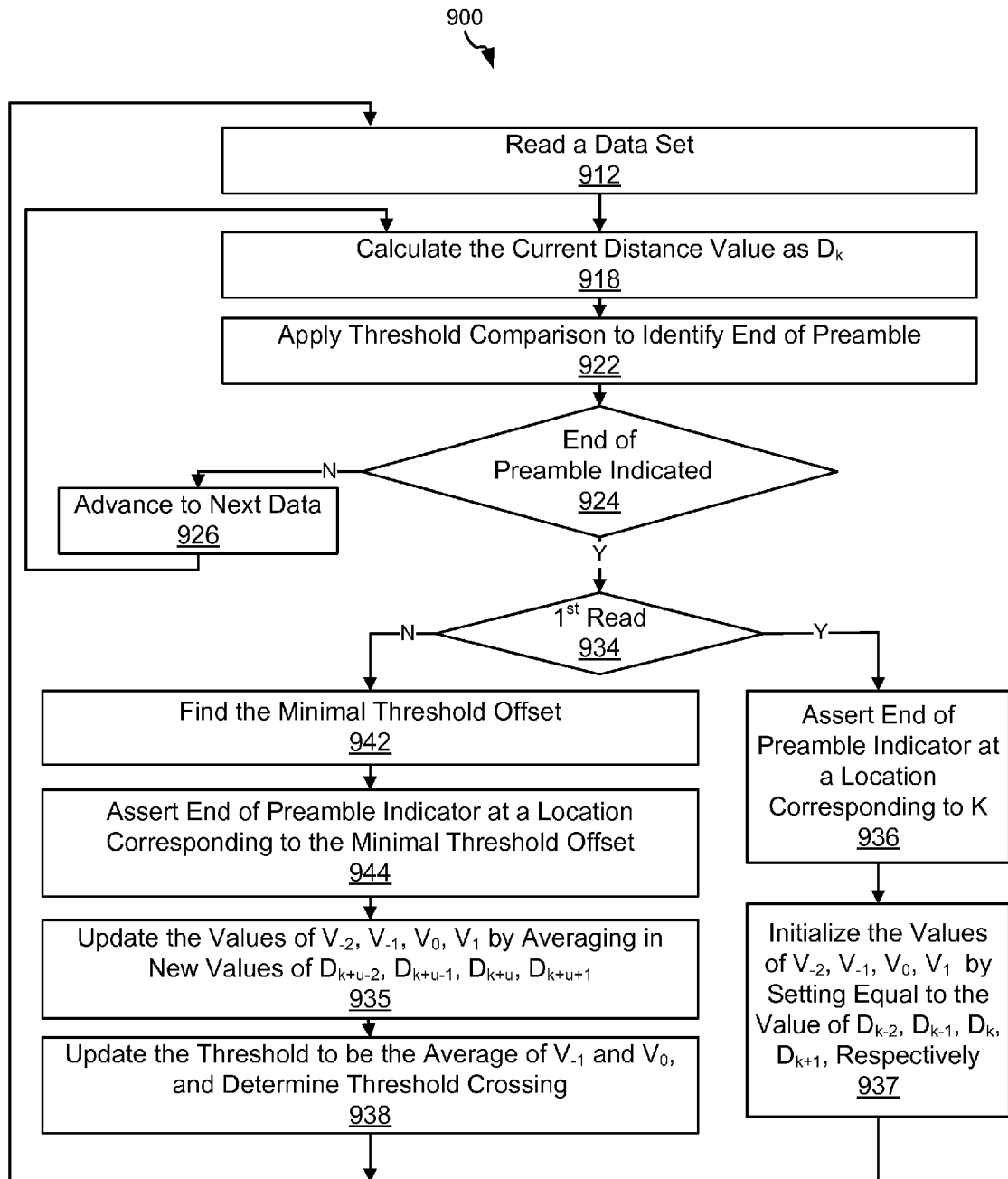


Fig. 9

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SYSTEMS AND METHODS FOR ENHANCED SYNC MARK MIS-DETECTION PROTECTION

CROSS REFERENCE TO RELATED APPLICATION

The present application claims priority to U.S. Pat. App. No. 61/785,947 entitled "Systems and Methods for Sync Mark Mis-Detection Protection" and filed on Mar. 14, 2013 by Yang. The entirety of the aforementioned reference is incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for detecting patterns in a data stream.

BACKGROUND OF THE INVENTION

Various circuits have been developed that provide for identifying synchronization marks within a data stream. As an example, a synchronization mark is identified based upon a threshold comparison. Such a threshold comparison approach depends highly upon determining an appropriate threshold for comparison. Where the selected threshold is too high, sync marks will be missed. Alternatively, where the selected threshold is too low, sync marks may be incorrectly identified. Either case is problematic for proper data processing.

Hence, for at least the aforementioned reasons, there exists a need in the art for advanced systems and methods for sync mark identification.

BRIEF SUMMARY OF THE INVENTION

The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for detecting patterns in a data stream.

Various embodiments of the present invention provide data processing systems that include: a first pattern identification circuit operable to identify a first pattern in a data set; a second pattern identification circuit operable to identify a second pattern in the data set; a distance calculation circuit operable to calculate a distance between the first pattern and the second pattern; and a quality output circuit operable to provide a quality metric corresponding to the distance between the first pattern and the second pattern.

This summary provides only a general outline of some embodiments of the invention. The phrases "in one embodiment," "according to one embodiment," "in various embodiments," "in one or more embodiments," "in particular embodiments" and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one embodiment of the present invention, and may be included in more than one embodiment of the present invention. Importantly, such phrases do not necessarily refer to the same embodiment. Many other embodiments of the invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

A further understanding of the various embodiments of the present invention may be realized by reference to the figures

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which are described in remaining portions of the specification. In the figures, like reference numerals are used throughout several figures to refer to similar components. In some instances, a sub-label consisting of a lower case letter is associated with a reference numeral to denote one of multiple similar components. When reference is made to a reference numeral without specification to an existing sub-label, it is intended to refer to all such multiple similar components.

FIG. 1 is a block diagram of a known magnetic storage medium and sector data scheme consistent with existing art;

FIG. 2 is a timing diagram showing an example of a sync mark detected within an allowable window in accordance with one or more embodiments of the present invention;

FIG. 3 is a timing diagram showing an example of assertion of a sync found signal beyond an expected window in accordance with one or more embodiments of the present invention;

FIG. 4a depicts a data processing circuit including a sync mark detection and framing circuit including mis-detection avoidance circuitry in accordance with some embodiments of the present invention;

FIG. 4b shows an example implementation of a sync mark detection and framing circuit including mis-detection avoidance circuitry in accordance with one or more embodiments of the present invention;

FIG. 5 is a timing diagram showing an example of assertion of a sync found signal beyond an expected window in accordance with other embodiments of the present invention;

FIG. 6a depicts a data processing circuit including a sync mark detection and framing circuit including enhanced mis-detection avoidance circuitry in accordance with some embodiments of the present invention;

FIG. 6b shows an example implementation of a sync mark detection and framing circuit including enhanced mis-detection avoidance circuitry in accordance with one or more embodiments of the present invention;

FIG. 7 shows a storage system including a sync mark mis-detection avoidance circuit in accordance with some embodiments of the present invention;

FIG. 8 depicts a communication system including a sync mark mis-detection avoidance circuit in accordance with different embodiments of the present invention; and

FIG. 9 is a flow diagram showing a method for jitter reduction related to location identification across multiple re-reads of a data set.

DETAILED DESCRIPTION OF THE INVENTION

The present inventions are related to systems and methods for data processing, and more particularly to systems and methods for detecting patterns in a data stream.

Various embodiments of the present invention provide data processing systems that include: a first pattern identification circuit operable to identify a first pattern in a data set; a second pattern identification circuit operable to identify a second pattern in the data set; a distance calculation circuit operable to calculate a distance between the first pattern and the second pattern; and a quality output circuit operable to provide a quality metric corresponding to the distance between the first pattern and the second pattern. In some instances of the aforementioned embodiments, the first pattern is an end of preamble pattern and the second pattern is a sync mark pattern. In such instances of the aforementioned embodiments, the system further includes a sync mark found circuit operable to assert a sync mark found signal based upon a combination of the quality metric and identification of the sync mark pattern. In some instances of the aforementioned embodiments, the

system is implemented as part of an integrated circuit. In one or more instances of the aforementioned embodiments, the system is implemented as part of a storage device.

In various instances of the aforementioned embodiments, the first pattern identification circuit includes a differential detection circuit including: a first distance calculation circuit operable to calculate a first distance between a data set and a known sync mark pattern; a second distance calculation circuit operable to calculate a second distance between the data set and a predefined pattern; a summation circuit operable to combine the first distance with the second distance to yield a combined distance; and a pattern indicator circuit operable to compare the combined distance with a threshold value and to assert a first pattern indicator corresponding to identification of the first pattern in a data set when the combined distance exceeds the threshold value. In some cases, the combining the first distance and the second distance by the summation circuit includes subtracting the first distance from the second distance to yield the combined distance.

In some instances of the aforementioned embodiments, the first pattern identification circuit includes a multiple sample latching circuit operable to store two or more locations of the first pattern in the data set across multiple reads of the data set. In some such instances, the multiple sample latching circuit is further operable to select one of the two or more locations based upon the two or more locations. In particular of such instances, the two or more locations are updated through an averaging process.

Other embodiments of the present invention provide data processing systems that include: a first pattern identification circuit operable to identify a maximal correlation value between a data set and a first pattern; a second pattern identification circuit operable to identify a second pattern in the data set; and a quality output circuit operable to provide a quality metric corresponding to the maximal correlation value. In some instances of the aforementioned embodiments, the first pattern is a preamble pattern and the second pattern is a sync mark pattern, and wherein the system further includes a sync mark found circuit operable to assert a sync mark found signal based upon a combination of the quality metric and identification of the sync mark pattern. In various instances of the aforementioned embodiments, the first pattern identification system includes a Euclidean distance calculation circuit operable to calculate a Euclidean distance between the first pattern and the data set, and the maximal correlation value occurs where the Euclidean distance is a minimum.

Various embodiments of the present invention provide data processing systems that include, a sync mark detection circuit, a distance calculation circuit, and a sync output circuit. The sync mark detection circuit is operable to identify a predefined pattern in a received data set, and to assert a sync found output when the predefined pattern is identified. The distance calculation circuit is operable to determine a distance from a preceding occurrence to assertion of the sync found output. The sync output circuit is operable to assert a sync mark detected output corresponding to the sync found output when the distance is less than a threshold value. In some cases, the threshold value is programmable. In various cases, the threshold value is greater than the length of the predefined pattern. In some cases, the received data set further includes a preamble pattern, and the preceding occurrence is a detected end of the preamble pattern. In some cases, the preamble pattern is a defined length. In some such cases, the defined length is greater than the length of the predefined pattern. In various instances of the aforementioned embodiments, the sync output circuit is further operable to assert a

mis-identified sync output when the sync found output is asserted when the distance is greater than the threshold value. In some cases, the system is implemented as part of an integrated circuit. In various cases, the system is implemented as part of a storage device or a wireless communication device.

In various instances of the aforementioned embodiments, the received data is derived from a user data region of a storage medium. In some cases, the preceding occurrence is within the user data region of the storage medium. In other cases, the preceding occurrence is within a servo data region of the storage medium, and wherein the servo data region directly precedes the user data region.

Other embodiments of the present invention provide data processing systems that include a sync mark detection circuit, and a sync quality output circuit. The sync mark detection circuit is operable to identify a predefined pattern in a received data set. Identification of the predefined pattern results in asserting a sync found output. A preamble pattern precedes the predefined pattern in the received data set. The sync quality output circuit is operable to provide a sync mark quality metric indicating a similarity between the preamble pattern and the received data set within a region preceding the predefined pattern. In some cases, the data processing system further includes a sync output circuit operable to assert a sync mark detected output corresponding to the sync found output when the sync mark quality metric is less than a threshold value. In other cases, the sync output circuit is further operable to assert a mis-identified sync output when the sync found output is asserted when a distance is greater than the threshold value.

Some embodiments of the present invention provide data processing systems that include: a first distance calculation circuit operable to calculate a first distance between a data input and a known sync mark pattern; a second distance calculation circuit operable to calculate a second distance between the data input and a predefined pattern; a summation circuit operable to combine the first distance with the second distance to yield a combined distance; and a sync quality output circuit operable to provide a sync mark quality metric indicating a similarity between the predefined pattern and the data input based at least in part on the combined distance. In some cases, the data processing systems further include an end of pattern detector circuit operable to compare the combined distance with a threshold value and to assert an end of pattern indicator when the combined distance exceeds the threshold value. In various instances of the aforementioned embodiments, the combining the first distance and the second distance by the summation circuit includes subtracting the first distance from the second distance to yield the combined distance.

In one or more instances of the aforementioned embodiments, the systems further include a maximum distance value register operable to maintain a maximum value of the combined distance occurring before the assertion a framing signal. In some cases, the maximum distance value register is set to a low value upon assertion of the framing signal. In various cases, the predefined pattern is a preamble pattern, and the sync quality output circuit includes: a third distance calculation circuit operable to calculate a third distance between the data input and a sync mark pattern; and a sync mark detection circuit operable to compare the third distance with a threshold value to yield the framing signal. The framing signal is asserted when the third distance is less than the threshold value. In some particular cases, the threshold is a first threshold, and the sync quality output circuit further includes a maximum distance comparator circuit operable to compare the maximum value with a second threshold. The sync mark

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quality metric indicates a likely valid sync mark when the maximum value is less than the second threshold, and the sync mark quality metric indicates a likely invalid sync mark when the maximum value is greater than the second threshold.

Turning to FIG. 1, a storage medium 1 is shown with two exemplary tracks 20, 22 indicated as dashed lines. The tracks are segregated by servo data written within wedges 19, 18. These wedges include servo data 10 that are used for control and synchronization of a read/write head assembly over a desired location on storage medium 1. In particular, the servo data generally includes a preamble pattern 11 followed by a servo address mark 12 (SAM). Servo address mark 12 is followed by a Gray code 13, and Gray code 13 is followed by burst information 14. It should be noted that while two tracks and two wedges are shown, hundreds of each would typically be included on a given storage medium. Further, it should be noted that a servo data set may have two or more fields of burst information. Yet further, it should be noted that different information may be included in the servo fields such as, for example, repeatable run-out information that may appear after burst information 14.

Between the servo data bit patterns 10a and 10b, a user data region 16 is provided. User data region 16 may include one or more sets of data that are stored to storage medium 1. The data sets may include user synchronization information some of which may be used as a mark to establish a point of reference from which processing of the data within user data region 16 may begin processing.

In operation, storage medium 1 is rotated in relation to a sensor that senses information from the storage medium. In a read operation, the sensor would sense servo data from wedge 19 (i.e., during a servo data period) followed by user data from a user data region between wedge 19 and wedge 18 (i.e., during a user data period) and then servo data from wedge 18. In a write operation, the sensor would sense servo data from wedge 19 then write data to the user data region between wedge 19 and wedge 18. Then, the sensor would be switched to sense a remaining portion of the user data region followed by the servo data from wedge 18. Once the user data region is reached, a user sync mark 50 is detected and used as a reference point from which data processing is performed. User sync mark 50 is preceded by a user preamble 51.

As used herein, the phrase “sync mark” is used in its broadest sense to mean any pattern that may be used to establish a point of reference. Thus, for example, a sync mark may be user sync mark 50 as is known in the art, or one or more portions of servo data bit patterns 10. Based upon the disclosure provided herein, one of ordinary skill in the art may recognize other sync marks that could be used in relation to different embodiments of the present invention.

It has been determined that some sync mark detection algorithms are prone to misidentifying non-sync mark data as a sync mark when the actual sync mark has been destroyed due to media defects or thermal asperity. One such sync mark detection algorithm is that discussed in U.S. patent application Ser. No. 12/946,048 entitled “Systems and Methods for Sync Mark Detection” and filed Nov. 15, 2010. The entirety of the aforementioned reference is incorporated herein for all purposes.

Further, it has been found that occasionally user data will include sufficient similarity to a sync mark to result in a false positive sync mark detection. Some embodiments of the present invention utilize a sync mark detection algorithm to identify a possible sync mark, but with a condition that the identified sync mark must occur within an acceptable range of a preceding occurrence. In some embodiments of the present

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invention, the preceding occurrence is an end of preamble identifier occurring at some point before a sync mark would be expected. This approach helps to avoid mis-detection of sync marks (i.e., false positives).

Turning to FIG. 2, a timing diagram 200 shows an example of a sync mark detected within an allowable window 250 in accordance with one or more embodiments of the present invention. Following timing diagram 200, a preamble pattern 210 including a number of repeating bit series is shown followed by a sync mark pattern 220. As shown, the repeating bit series is a 2T series (i.e., ‘1100’). Based upon the disclosure provided herein, one of ordinary skill in the art will recognize other repeating patterns that may be used in relation to different embodiments of the present invention.

An end of preamble signal 230 is asserted after the last of the repeating bit series are detected. In some embodiments of the present invention, the end of preamble signal 230 is detected by an end of preamble detector circuit that calculates a Euclidean distance between a defined number of bits of received data 205. In some embodiments of the present invention, the defined number of bits of received data 205 is twenty (20). The Euclidean distance is calculated in accordance with the following equation:

Euclidean Distance =

$$\sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownPreamblePattern}[k])^2,$$

where k indicates a particular bit pair being compared, and received data 205 and the preamble pattern are assumed to be aligned. Where received data 205 is error free, the calculated Euclidean distance will be zero when preamble pattern 210 is being received as received data 205, and will increase dramatically when a sync mark pattern 220 begins to be received as received data 205. Where preamble pattern 210 is not noiseless, the calculated value of the Euclidean distance will be greater than zero. However, where the noise is not overwhelming to the signal, the calculated value of the Euclidean distance will still increase detectably between the transition from preamble pattern 210 to a sync mark pattern 220. Once the calculated Euclidean distance exceeds an EOP threshold value, end of preamble signal 230 is asserted as a logic ‘1’. The location where end of preamble signal 230 is asserted is referred to as “L1”.

A known sync mark pattern is also compared against received data 205, and a sync found signal 240 is asserted as a logic ‘1’ when a match is detected. In one embodiment of the present invention, a Euclidean distance between sync mark pattern 220 and a known sync mark pattern is calculated in accordance with the following equation:

Euclidean Distance =

$$\sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownSyncMarkPattern}[k])^2,$$

where k indicates a particular bit pair being compared. Where the calculated Euclidean distance is less than an SM threshold value, sync found signal 240 is asserted as a logic ‘1’. The

location where sync found signal **240** is asserted is referred to as “L2”. Where L2–L1 (represented by a distance **260**) is less than or equal to an expected distance threshold (represented by an allowable window distance **250**), sync mark found signal **240** is accepted as correct. Alternatively, where L2–L1 (represented by distance **260**) is greater than the expected distance threshold (represented by allowable window distance **250**), sync found signal **240** is identified as unreliable and may be used or rejected depending upon an implemented processing algorithm. In some cases, assertion of sync mark found signal **240** may be suppressed where it is identified as unreliable. In other cases, assertion of sync mark found signal **240** occurs along with an indication that it may not be reliable. In such a way, mis-detection may be avoided or at least the potential of mis-detection flagged.

In some embodiments of the present invention, the distance L2–L1 is replaced with a soft metric, $D[k]_{\max}$, that corresponds a maximum Euclidean distance that occurs prior to the syncmark pattern location, where the location of the sync mark pattern is indicated by sync found signal **240** in accordance with the following equation:

$$D[k]_{\max} = \text{MAX} \left[\sum_{k=0}^{19} (ReceivedData[k] - KnownPreamblePattern[k])^2 \right].$$

This soft metric is then compared with an expected distance threshold such that where the threshold is exceeded it is determined that the probability of detecting a false sync mark is significant and the asserted sync mark found signal **240** may be unreliable. In some cases, assertion of sync mark found signal **240** may be suppressed where it is identified as unreliable. In other cases, assertion of sync mark found signal **240** occurs along with an indication that it may not be reliable. In such a way, mis-detection may be avoided or at least the potential of mis-detection flagged.

Turning to FIG. 3, a timing diagram **300** shows an example of assertion of a sync found signal **340** beyond an expected window **360**. Following timing diagram **300**, a received data **305** includes a preamble pattern **310**, an actual noise corrupted sync mark **320**, and user data **380**. The user data **380** includes a sync mark like pattern **390** that begins a distance **385** from the beginning of actual noise corrupted sync mark **320**. As described above in relation to FIG. 2, it is expected that preamble pattern **310** include a number of repeating bit series that are followed by a valid sync mark pattern. However, in this case, the sync mark pattern is noisy resulting in a failed detection (i.e., a failure to assert sync found signal **340** as a logic ‘1’). Sync mark like pattern **390** is not an intended sync mark, but rather a pattern within user data **380** that sufficiently resembles a sync mark pattern that it results in assertion of sync found signal **340**.

Similar to that described above in relation to FIG. 2, an end of preamble signal **330** is asserted after the last of the repeating bit series are detected. In some embodiments of the present invention, the end of preamble signal **330** is detected by an end of preamble detector circuit that calculates a Euclidean distance between a defined number of bits of received data **305**. In some embodiments of the present invention, the defined number of bits of received data **305** is twenty (20).

A differential Euclidean distance ($D[k]$) is calculated in accordance with the following equation:

$$D[k] = \text{Euclidean Distance} =$$

$$\sum_{k=0}^{19} (ReceivedData[k] - KnownPreamblePattern[k])^2 - \sum_{k=0}^{19} (ReceivedData[k] - KnownSyncMarkPattern[k])^2,$$

where k indicates a particular bit pair being compared, and received data **305** and the preamble pattern are assumed to be aligned. The differential Euclidean distance value is described in more detail below in relation to FIG. 6a. The Euclidean distance ($D[k]$) is shown on timing diagram **300** as $D[k]$ **370**. Where received data **305** is error free and a preamble pattern is being received, $D[k]$ **370** will be less than zero as the first term in the equation will be zero, and the second term in the equation will be non-zero. As shown, $D[k]$ **370** increases dramatically at the transition between preamble **310** and the subsequent field (i.e., actual noise corrupted sync mark **320**) of received data **305**. The value of $D[k]$ **370** will vary as actual noise corrupted sync mark **320** and user data **380** is received. An example metric **375** is shown where a maximum value of $D[k]$ **370** is achieved at a distance **397** from assertion of end of preamble signal **330**. Said another way, $D[k]_{\max}$ occurs distance **397** from assertion of end of preamble signal **330**. Metric **375** is used as an indication of the validity of sync found signal **340**. In particular, the excessive value of metric **375** suggests that there is non-preamble data between end of preamble **330** and sync found signal **340** which suggests that sync found signal **340** is a specious assertion. Alternatively, where the value of metric **375** is not as large, it is an indication that the data between end of preamble **330** and sync found signal **340** is more likely to be preamble data and thus sync found signal **340** may represent an actual sync mark.

A known sync mark pattern is also compared against received data **305**, and sync found signal **340** is asserted as a logic ‘1’ when a match is detected. In one embodiment of the present invention, a Euclidean distance between received data **305** and a known sync mark pattern is calculated in accordance with the following equation:

$$\text{Euclidean Distance} =$$

$$\sum_{k=0}^{19} (ReceivedData[k] - KnownSyncMarkPattern[k])^2,$$

where k indicates a particular bit pair being compared. Where the calculated Euclidean distance is less than an SM threshold value, sync found signal **340** is asserted as a logic ‘1’. As previously noted, because of the corruption of actual noise corrupted sync mark **320**, the calculated Euclidean distance is always greater than the SM threshold resulting in a failure to assert sync found signal **340** as a logic ‘1’, but later the calculated Euclidean distance goes below the SM threshold coincident with receiving sync mark like pattern **390** resulting in assertion of sync found signal **340** as a logic ‘1’. This assertion of sync found signal **340** as a logic ‘1’ occurs a distance **399** from assertion of end of preamble signal **330**.

Turning to FIG. 4a, a data processing circuit 400 including a sync mark detection and framing circuit having sync mark mis-detection circuitry is shown in accordance with some embodiments of the present invention. Of note, the received data discussed in FIGS. 2-3 above corresponds to an equalized output 422 in data processing system 400. Data processing circuit 400 includes an analog front end circuit 410 that receives an analog input 408. Analog front end circuit 410 processes analog input 408 and provides a processed analog signal 412 to an analog to digital converter circuit 415. Analog front end circuit 410 may include, but is not limited to, an analog filter and an amplifier circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuitry that may be included as part of analog front end circuit 410. In some cases, analog input 408 is derived from a read/write head assembly (not shown) that is disposed in relation to a storage medium (not shown). In other cases, analog input 408 is derived from a receiver circuit (not shown) that is operable to receive a signal from a transmission medium (not shown). The transmission medium may be wired or wireless. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of sources from which analog input 408 may be derived.

Analog to digital converter circuit 415 converts processed analog signal 412 into a corresponding series of digital samples 417. Analog to digital converter circuit 415 may be any circuit known in the art that is capable of producing digital samples corresponding to an analog input signal. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of analog to digital converter circuits that may be used in relation to different embodiments of the present invention. Digital samples 417 are provided to an equalizer circuit 420. Equalizer circuit 420 applies an equalization algorithm to digital samples 417 to yield equalized output 422. In some embodiments of the present invention, equalizer circuit 420 is a digital finite impulse response filter circuit as are known in the art.

Equalized output 422 is provided to a data detector circuit 425, a sample buffer circuit 475, and a sync mark detection and framing circuit 490. Sync mark detection and framing circuit 490 includes mis-detection avoidance circuitry that operates similar to that discussed above in relation to FIGS. 2-3. In particular, sync mark detection and framing circuit 490 compares equalized output 422 against a known preamble pattern. In one particular embodiment of the present invention, the comparison is achieved by calculating a distance value (D[k]) in accordance with the following equation:

$$D[k] = \text{Euclidean Distance} =$$

$$\sum_{k=0}^{19} (\text{EqualizedOutput}[k] - \text{KnownPreamblePattern}[k])^2,$$

where k indicates a particular bit pair being compared, and equalized output 422 and the known preamble pattern are aligned. Where equalized output 422 is error free, the distance value (D[k]) will be zero, and will have a relatively low value where the signal is not overwhelmed by the noise. When equalized output 422 transitions from the preamble pattern to the next field (expected to be the sync mark pattern), the distance value increases dramatically. The distance value will vary as non-preamble fields are received. Once the expected number of preamble packets have been received, an end of preamble signal is asserted.

A known sync mark pattern is also compared against equalized output 422, and a framing signal (i.e., a sync mark found signal) 493 is asserted as a logic '1' when a match is detected. In one embodiment of the present invention, the comparison between equalized output 422 and the known sync mark pattern may be done by calculating a Euclidean distance between equalized output 422 and the known sync mark pattern in accordance with the following equation:

$$\text{Euclidean Distance} =$$

$$\sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownSyncMarkPattern}[k])^2,$$

where k indicates a particular bit pair being compared. This Euclidean distance is compared with an SM threshold value, and where it is smaller than the SM threshold value, framing signal 493 is asserted as a logic '1'. Otherwise, framing signal 493 is not asserted. In some cases, the SM threshold value is a user programmed value. In other cases, the SM threshold value is a fixed value.

In addition, the distance value calculated as part of comparing equalized output 422 for each calculation period between assertion of the end of preamble signal and subsequent assertion of framing signal 493 are compared with an expected distance value. In some cases, the expected distance value is a user programmed value. In other cases, the expected distance value is a fixed value. Where the distance value is greater than the expected distance value, a sync reliability signal 497 is asserted to indicate the assertion of framing signal 493 may be unreliable. This reliability information may be used to either suppress the assertion of framing signal 493, or provided to a host (not shown) or error checking circuit (not shown) where it is used as an indication of a processing failure and/or in providing retry processing. In such a way, mis-detection may be avoided or at least the potential of mis-detection flagged. The aforementioned distance value and/or sync reliability output 497 may be more generically referred to as an example of a sync mark quality metric.

Sample buffer circuit 475 stores equalized output 422 as buffered data 477 for use in subsequent iterations through data detector circuit 425. Data detector circuit 425 may be any data detector circuit known in the art that is capable of producing a detected output 427. As some examples, data detector circuit 425 may be, but is not limited to, a Viterbi algorithm detector circuit or a maximum a posteriori detector circuit as are known in the art. Of note, the general phrases "Viterbi data detection algorithm" or "Viterbi algorithm data detector circuit" are used in their broadest sense to mean any Viterbi detection algorithm or Viterbi algorithm detector circuit or variations thereof including, but not limited to, bi-direction Viterbi detection algorithm or bi-direction Viterbi algorithm detector circuit. Also, the general phrases "maximum a posteriori data detection algorithm" or "maximum a posteriori data detector circuit" are used in their broadest sense to mean any maximum a posteriori detection algorithm or detector circuit or variations thereof including, but not limited to, simplified maximum a posteriori data detection algorithm and a max-log maximum a posteriori data detection algorithm, or corresponding detector circuits. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detector circuits that may be used in relation to different embodiments of the present invention. Detected output 425 may include both hard decisions and soft

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decisions. The terms “hard decisions” and “soft decisions” are used in their broadest sense. In particular, “hard decisions” are outputs indicating an expected original input value (e.g., a binary ‘1’ or ‘0’, or a non-binary digital value), and the “soft decisions” indicate a likelihood that corresponding hard decisions are correct. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of hard decisions and soft decisions that may be used in relation to different embodiments of the present invention. Data detector circuit 425 uses framing signal 493 to determine the beginning point of codewords accessed from sample buffer circuit 475 for processing.

Detected output 427 is provided to a central queue memory circuit 460 that operates to buffer data passed between data detector circuit 425 and data decoder circuit 450. In some cases, central queue memory circuit 460 includes interleaving (i.e., data shuffling) and de-interleaving (i.e., data un-shuffling) circuitry known in the art. When data decoder circuit 450 is available, data decoder circuit 450 accesses detected output 427 from central queue memory circuit 460 as a decoder input 456. Data decoder circuit 450 applies a data decoding algorithm to decoder input 456 in an attempt to recover originally written data. The result of the data decoding algorithm is provided as a decoded output 452. Similar to detected output 427, decoded output 452 may include both hard decisions and soft decisions. For example, data decoder circuit 450 may be any data decoder circuit known in the art that is capable of applying a decoding algorithm to a received input. Data decoder circuit 450 may be, but is not limited to, a low density parity check (LDPC) decoder circuit or a Reed Solomon decoder circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data decoder circuits that may be used in relation to different embodiments of the present invention. Where the original data is recovered (i.e., the data decoding algorithm converges) or a timeout condition occurs, decoded output 452 is stored to a memory included in a hard decision output circuit 480. In turn, hard decision output circuit 480 provides the converged decoded output 452 as a data output 484 to a recipient (not shown). The recipient may be, for example, an interface circuit operable to receive processed data sets. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of recipients that may be used in relation to different embodiments of the present invention. Where the original data is not recovered (i.e., the data decoding algorithm failed to converge) prior to a timeout condition, decoded output 452 indicates that the data is unusable as is more specifically discussed below, and data output 484 is similarly identified as unusable.

Data decoder circuit 453 additionally provides a framing signal selection signal 453 to sync mark detection and framing circuit 490 that causes sync mark detection and framing circuit 490 to provide a next best framing signal 493. Equalized output 422 is then re-processed using the new framing signal 493 indicating a different starting location of user data in equalized output 422. In some embodiments of the present invention, framing signal selection signal 453 is asserted to cause another framing signal to be provided under particular conditions. Such conditions may include, for example, a failure of data decoder circuit 450 to converge after a defined number of global iterations, and/or where a number of unsatisfied checks exceed a defined level after a defined number of global iterations have occurred in relation to the currently processing data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety

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of conditions upon which a next best framing signal is selected to restart the processing.

One or more iterations through the combination of data detector circuit 425 and data decoder circuit 450 may be made in an effort to converge on the originally written data set. As mentioned above, processing through both the data detector circuit and the data decoder circuit is referred to as a “global iteration”. For the first global iteration, data detector circuit 425 applies the data detection algorithm to equalized output 422 without guidance from a decoded output. For subsequent global iterations, data detector circuit 425 applies the data detection algorithm to buffered data 477 as guided by decoded output 452. To facilitate this guidance, decoded output 452 is stored to central queue memory circuit 460 as a decoder output 454, and is provided from central queue memory circuit 460 as a detector input 429 when equalized output 422 is being re-processed through data detector circuit 425.

During each global iteration it is possible for data decoder circuit 450 to make one or more local iterations including application of the data decoding algorithm to decoder input 456. For the first local iteration, data decoder circuit 450 applies the data decoder algorithm without guidance from decoded output 452. For subsequent local iterations, data decoder circuit 450 applies the data decoding algorithm to decoder input 456 as guided by a previous decoded output 452. The number of local iterations allowed may be, for example, ten. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of different numbers of local iterations that may be allowed in accordance with different embodiments of the present invention. Where the number of local iterations through data decoder circuit 450 exceeds that allowed, but it is determined that at least one additional global iteration during standard processing of the data set is allowed, decoded output 452 is provided back to central queue memory circuit 460 as decoded output 454. Decoded output 454 is maintained in central queue memory circuit 460 until data detector circuit 425 becomes available to perform additional processing.

In contrast, where the number of local iterations through data decoder circuit 450 exceeds that allowed and it is determined that the allowable number of global iterations has been surpassed for the data set and/or a timeout or memory usage calls for termination of processing of the particular data set, standard processing of the data set concludes and an error is indicated. In some cases, retry processing or some offline processing may be applied to recover the otherwise unconverged data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of non-standard processing techniques that may be applied to recover the otherwise unrecoverable data set.

Turning to FIG. 4b, an example implementation of a sync mark detection and framing circuit 790 including mis-detection avoidance circuitry is shown in accordance with one or more embodiments of the present invention. Sync mark detection and framing circuit 790 may be used in place of sync mark detection and framing circuit 490 discussed above in relation to FIG. 4a where an input 705 is connected to equalized output 422, a framing signal 757 is connected to framing signal 493, and a sync reliability signal 787 is connected to sync reliability signal 497. Distance 767 and/or sync reliability signal 787 may be more generically referred to as an example of a sync mark quality metric.

As shown, sync mark detection and framing circuit 790 includes a distance calculation circuit 720 operable to calcu-

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late a distance (D[k]) 722 between input 705 and a known preamble pattern 710 in accordance with the following equation:

$$D[k] = \text{Euclidean Distance} = \sum_{k=0}^{19} (\text{Input}[k] - \text{KnownPreamblePattern}[k])^2,$$

where k indicates a particular bit pair being compared, and input 705 and the known preamble pattern are aligned. Where input 705 is error free, distance (D[k]) 722 will be zero, and distance (D[k]) 722 will have a relatively low value where the signal of input 705 is not overwhelmed by the noise. When input 705 transitions from the preamble pattern to the next field (expected to be the sync mark pattern), distance (D[k]) 722 increases dramatically. Distance (D[k]) 722 will vary as non-preamble fields are received. Distance (D[k]) 722 is provided to an end of preamble detection circuit 770 that asserts an end of preamble signal 777 when the end of a preamble is identified.

In addition, distance (D[k]) 722 is provided to a maximum distance value register circuit 760 that is operable to compare distance (D[k]) 722 with a previously stored distance value 767 to determine which is greater, and to retain the greater of the two as distance value 767. The distance value 767 stored in maximum distance value register circuit 760 is set equal to zero when framing signal 757 is asserted indicating that a sync mark was found. Distance value 767 is provided to a maximum distance comparator circuit 780 where it is compared with an expected distance threshold 789. Expected distance threshold 789 may be either fixed or user programmable. Where distance value 767 is greater than expected distance threshold 789, maximum distance comparator circuit 780 asserts sync reliability signal 787 to indicate that a subsequent assertion of framing signal 757 is unreliable. In some cases, distance (D[k]) 722 is only accumulated prior to the syncmark pattern. Such accumulation could be a few cycles before the assertion of the syncmark found signal. For example, if the syncmark length is twenty (20), then the accumulation may only accumulate the maximal distance metric five (5) cycles prior to syncmark being found.

In addition, a distance calculation circuit 740 calculates a distance 742 between input 705 and a known sync mark pattern 730 in accordance with the following equation:

$$\text{Distance} = \sum_{k=0}^{19} (\text{Input}[k] - \text{KnownSyncMarkPattern}[k])^2,$$

where k indicates a particular bit pair being compared. Distance 742 is provided to a sync mark detection circuit 750 that is operable to compare distance 742 with an SM threshold 759. SM threshold 759 may be either fixed or user programmable. Where distance 742 is less than SM threshold value 759, framing signal 757 is asserted to indicate that a sync mark signal has been found.

Turning to FIG. 5, a timing diagram 500 shows another example of assertion of a sync found signal beyond an expected window in accordance with other embodiments of the present invention. Timing diagram 500 is similar to timing diagram 200 described in relation to FIG. 3 above, except that the transition of a Euclidian distance (D[k]) 570 (shown as a solid line curve 571) is substantially steeper than that of Euclidian distance (D[k]) 370 (shown as a dashed line curve

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573) of FIG. 3. This increase in the abruptness of the transition enhances the repeatability of end of preamble detection, and is achieved by using a different algorithm than that used to achieve the result of FIG. 3.

Following timing diagram 500, a received data 505 includes a preamble pattern 510, an actual noise corrupted sync mark 520, and user data 580. The user data 580 includes a sync mark like pattern 590 that begins a distance 585 from the beginning of actual noise corrupted sync mark 520. As described above in relation to FIG. 2, it is expected that preamble pattern 510 include a number of repeating bit series that are followed by a valid sync mark pattern. However, in this case, the sync mark pattern is noisy resulting in a failed detection (i.e., a failure to assert sync found signal 540 as a logic '1'). Sync mark like pattern 590 is not an intended sync mark, but rather a pattern within user data 580 that sufficiently resembles a sync mark pattern that it results in assertion of sync found signal 540.

Similar to that described above in relation to FIG. 2, an end of preamble signal 530 is asserted after the last of the repeating bit series are detected. In some embodiments of the present invention, the end of preamble signal 530 is detected by an end of preamble detector circuit that calculates a Euclidean distance between a defined number of bits of received data 505. In some embodiments of the present invention, the defined number of bits of received data 505 is twenty (20). The Euclidean distance (D[k]) is calculated in accordance with the following equation:

$$D[k] = \text{Euclidean Distance} =$$

$$\sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownPreamblePattern}[k])^2 - \sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownSyncMarkPattern}[k])^2,$$

where k indicates a particular bit pair being compared, and received data 505, the preamble pattern, and the known sync mark pattern are all assumed to be aligned. The Euclidian distance (D[k]) is shown on timing diagram 500 as D[k] 570. As mentioned above, the preceding algorithm yields a more abrupt transition (i.e., solid line curve 571) than that achieved by the following algorithm used to achieve a less abrupt transition (i.e., dashed line curve 573):

$$D[k] = \text{Euclidean Distance} =$$

$$\sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownPreamblePattern}[k])^2.$$

Where received data 505 is error free and a preamble pattern is being received, D[k] 570 will be less than zero as the first term in the equation will be zero, and the second term in the equation will be non-zero. As shown, D[k] 570 increases dramatically (shown as solid line curve 571) at the transition between preamble 510 and the subsequent field (i.e., actual noise corrupted sync mark 520) of received data 505. The value of D[k] 570 will vary as actual noise corrupted sync mark 520 and user data 580 is received. An example metric 575 is shown where a maximum value of D[k] 570 is achieved at a distance 597 from assertion of end of preamble signal

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530. Said another way, D[k]max occurs distance 597 from assertion of end of preamble signal 530.

A known sync mark pattern is also compared against received data 505, and sync found signal 540 is asserted as a logic '1' when a match is detected. In one embodiment of the present invention, a Euclidean distance between received data 505 and a known sync mark pattern is calculated in accordance with the following equation:

Euclidean Distance =

$$\sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownSyncMarkPattern}[k])^2,$$

where k indicates a particular bit pair being compared. Where the calculated Euclidean distance is less than an SM threshold value, sync found signal 540 is asserted as a logic '1'. As previously noted, because of the corruption of actual noise corrupted sync mark 520, the calculated Euclidean distance is always greater than the SM threshold resulting in a failure to assert sync found signal 540 as a logic '1', but later the calculated Euclidean distance goes below the SM threshold coincident with receiving sync mark like pattern 590 resulting in assertion of sync found signal 540 as a logic '1'. This assertion of sync found signal 540 as a logic '1' occurs a distance 599 from assertion of end of preamble signal 530. In this case, the value of example metric 575 is greater than an expected distance threshold and the location of example metric (i.e., distance 597) is closer to the assertion of end of preamble signal 530 than the location of sync found signal 540 (i.e., distance 599), the assertion of sync found signal 540 is identified as unreliable and may be used or rejected depending upon an implemented processing algorithm. In some cases, assertion of sync mark found signal 540 may be suppressed where it is identified as unreliable. In other cases, assertion of sync mark found signal 540 occurs along with an indication that it may not be reliable. In such a way, mis-detection may be avoided or at least the potential of mis-detection flagged.

Turning to FIG. 6a, a data processing circuit 600 including a sync mark detection and framing circuit including enhanced mis-detection circuitry is shown in accordance with some embodiments of the present invention. Data processing circuit 600 includes an analog front end circuit 610 that receives an analog input 608. Analog front end circuit 610 processes analog input 608 and provides a processed analog signal 612 to an analog to digital converter circuit 615. Analog front end circuit 610 may include, but is not limited to, an analog filter and an amplifier circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuitry that may be included as part of analog front end circuit 610. In some cases, analog input 608 is derived from a read/write head assembly (not shown) that is disposed in relation to a storage medium (not shown). In other cases, analog input 608 is derived from a receiver circuit (not shown) that is operable to receive a signal from a transmission medium (not shown). The transmission medium may be wired or wireless. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of sources from which analog input 608 may be derived.

Analog to digital converter circuit 615 converts processed analog signal 612 into a corresponding series of digital samples 617. Analog to digital converter circuit 615 may be any circuit known in the art that is capable of producing

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digital samples corresponding to an analog input signal. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of analog to digital converter circuits that may be used in relation to different embodiments of the present invention. Digital samples 617 are provided to an equalizer circuit 620. Equalizer circuit 620 applies an equalization algorithm to digital samples 617 to yield an equalized output 622. In some embodiments of the present invention, equalizer circuit 620 is a digital finite impulse response filter circuit as are known in the art.

Equalized output 622 is provided to a data detector circuit 625, a sample buffer circuit 675, and a sync mark detection and framing circuit 690. Sync mark detection and framing circuit 690 includes enhanced mis-detection avoidance circuitry that operates similar to that discussed above in relation to FIG. 5. In particular, sync mark detection and framing circuit 690 compares equalized output 622 against a combination of a known preamble pattern and a known sync mark pattern. In one particular embodiment of the present invention, the comparison is achieved by calculating a distance value (D[k]) in accordance with the following equation:

D[k] = Euclidean Distance =

$$\sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownPreamblePattern}[k])^2 - \sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownSyncMarkPattern}[k])^2,$$

where k indicates a particular bit pair being compared, and equalized output 622 and the known preamble pattern are aligned. Where equalized output 622 is error free and a preamble pattern is being received, the Euclidean distance value (D[k]) will be less than zero as the first term in the equation will be zero, and the second term in the equation will be non-zero. When equalized output 622 transitions from the preamble pattern to the next field (expected to be the sync mark pattern), the distance value increases dramatically. The distance value will vary as non-preamble fields are received. Once the expected number of preamble packets have been received, an end of preamble signal is asserted.

A known sync mark pattern is also compared against equalized output 622, and a framing signal (i.e., a sync mark found signal) 693 is asserted as a logic '1' when a match is detected. In one embodiment of the present invention, the comparison between equalized output 622 and the known sync mark pattern may be done by calculating a Euclidean distance between equalized output 622 and the known sync mark pattern in accordance with the following equation:

Euclidean Distance =

$$\sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownSyncMarkPattern}[k])^2,$$

where k indicates a particular bit pair being compared. This Euclidean distance is compared with an SM threshold value, and where it is smaller than the SM threshold value, framing signal 693 is asserted as a logic '1'. Otherwise, framing signal 693 is not asserted. In some cases, the SM threshold value is a user programmed value. In other cases, the SM threshold value is a fixed value.

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In addition, the distance value calculated as part of comparing equalized output **622** for each calculation period between assertion of the end of preamble signal and subsequent assertion of framing signal **693** are compared with an expected distance value. In some cases, the expected distance value is a user programmed value. In other cases, the expected distance value is a fixed value. Where the distance value is greater than the expected distance value, a sync reliability signal **697** is asserted to indicate the assertion of framing signal **693** may be unreliable. This reliability information may be used to either suppress the assertion of framing signal **693**, or provided to a host (not shown) or error checking circuit (not shown) where it is used as an indication of a processing failure and/or in providing retry processing. In such a way, mis-detection may be avoided or at least the potential of mis-detection flagged. The aforementioned distance value and/or sync reliability output **697** may be more generically referred to as an example of a sync mark quality metric.

Sample buffer circuit **675** stores equalized output **622** as buffered data **677** for use in subsequent iterations through data detector circuit **625**. Data detector circuit **625** may be any data detector circuit known in the art that is capable of producing a detected output **627**. As some examples, data detector circuit **625** may be, but is not limited to, a Viterbi algorithm detector circuit or a maximum a posteriori detector circuit as are known in the art. Of note, the general phrases “Viterbi data detection algorithm” or “Viterbi algorithm data detector circuit” are used in their broadest sense to mean any Viterbi detection algorithm or Viterbi algorithm detector circuit or variations thereof including, but not limited to, bi-direction Viterbi detection algorithm or bi-direction Viterbi algorithm detector circuit. Also, the general phrases “maximum a posteriori data detection algorithm” or “maximum a posteriori data detector circuit” are used in their broadest sense to mean any maximum a posteriori detection algorithm or detector circuit or variations thereof including, but not limited to, simplified maximum a posteriori data detection algorithm and a max-log maximum a posteriori data detection algorithm, or corresponding detector circuits. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detector circuits that may be used in relation to different embodiments of the present invention. Detected output **625** may include both hard decisions and soft decisions. The terms “hard decisions” and “soft decisions” are used in their broadest sense. In particular, “hard decisions” are outputs indicating an expected original input value (e.g., a binary ‘1’ or ‘0’, or a non-binary digital value), and the “soft decisions” indicate a likelihood that corresponding hard decisions are correct. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of hard decisions and soft decisions that may be used in relation to different embodiments of the present invention. Data detector circuit **625** uses framing signal **693** to determine the beginning point of codewords accessed from sample buffer circuit **675** for processing.

Detected output **627** is provided to a central queue memory circuit **660** that operates to buffer data passed between data detector circuit **625** and data decoder circuit **650**. In some cases, central queue memory circuit **660** includes interleaving (i.e., data shuffling) and de-interleaving (i.e., data un-shuffling) circuitry known in the art. When data decoder circuit **650** is available, data decoder circuit **650** accesses detected output **627** from central queue memory circuit **660** as a decoder input **656**. Data decoder circuit **650** applies a data decoding algorithm to decoder input **656** in an attempt to recover originally written data. The result of the data decod-

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ing algorithm is provided as a decoded output **652**. Similar to detected output **627**, decoded output **652** may include both hard decisions and soft decisions. For example, data decoder circuit **650** may be any data decoder circuit known in the art that is capable of applying a decoding algorithm to a received input. Data decoder circuit **650** may be, but is not limited to, a low density parity check (LDPC) decoder circuit or a Reed Solomon decoder circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data decoder circuits that may be used in relation to different embodiments of the present invention. Where the original data is recovered (i.e., the data decoding algorithm converges) or a timeout condition occurs, decoded output **652** is stored to a memory included in a hard decision output circuit **680**. In turn, hard decision output circuit **680** provides the converged decoded output **652** as a data output **684** to a recipient (not shown). The recipient may be, for example, an interface circuit operable to receive processed data sets. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of recipients that may be used in relation to different embodiments of the present invention. Where the original data is not recovered (i.e., the data decoding algorithm failed to converge) prior to a timeout condition, decoded output **652** indicates that the data is unusable as is more specifically discussed below, and data output **684** is similarly identified as unusable.

Data decoder circuit **653** additionally provides a framing signal selection signal **653** to sync mark detection and framing circuit **690** that causes sync mark detection and framing circuit **690** to provide a next best framing signal **693**. Equalized output **622** is then re-processed using the new framing signal **693** indicating a different starting location of user data in equalized output **622**. In some embodiments of the present invention, framing signal selection signal **653** is asserted to cause another framing signal to be provided under particular conditions. Such conditions may include, for example, a failure of data decoder circuit **650** to converge after a defined number of global iterations, and/or where a number of unsatisfied checks exceed a defined level after a defined number of global iterations have occurred in relation to the currently processing data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of conditions upon which a next best framing signal is selected to restart the processing.

One or more iterations through the combination of data detector circuit **625** and data decoder circuit **650** may be made in an effort to converge on the originally written data set. As mentioned above, processing through both the data detector circuit and the data decoder circuit is referred to as a “global iteration”. For the first global iteration, data detector circuit **625** applies the data detection algorithm to equalized output **622** without guidance from a decoded output. For subsequent global iterations, data detector circuit **625** applies the data detection algorithm to buffered data **677** as guided by decoded output **652**. To facilitate this guidance, decoded output **652** is stored to central queue memory circuit **660** as a decoder output **654**, and is provided from central queue memory circuit **660** as a detector input **629** when equalized output **622** is being re-processed through data detector circuit **625**.

During each global iteration it is possible for data decoder circuit **650** to make one or more local iterations including application of the data decoding algorithm to decoder input **656**. For the first local iteration, data decoder circuit **650** applies the data decoder algorithm without guidance from decoded output **652**. For subsequent local iterations, data

decoder circuit 650 applies the data decoding algorithm to decoder input 656 as guided by a previous decoded output 652. The number of local iterations allowed may be, for example, ten. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of different numbers of local iterations that may be allowed in accordance with different embodiments of the present invention. Where the number of local iterations through data decoder circuit 650 exceeds that allowed, but it is determined that at least one additional global iteration during standard processing of the data set is allowed, decoded output 652 is provided back to central queue memory circuit 660 as decoded output 654. Decoded output 654 is maintained in central queue memory circuit 660 until data detector circuit 625 becomes available to perform additional processing.

In contrast, where the number of local iterations through data decoder circuit 650 exceeds that allowed and it is determined that the allowable number of global iterations has been surpassed for the data set and/or a timeout or memory usage calls for termination of processing of the particular data set, standard processing of the data set concludes and an error is indicated. In some cases, retry processing or some offline processing may be applied to recover the otherwise unconverged data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of non-standard processing techniques that may be applied to recover the otherwise unrecoverable data set.

Turning to FIG. 6b, an example implementation of a sync mark detection and framing circuit 791 including enhanced mis-detection avoidance circuitry is shown in accordance with one or more embodiments of the present invention. Sync mark detection and framing circuit 791 may be used in place of sync mark detection and framing circuit 690 discussed above in relation to FIG. 6a where an input 706 is connected to equalized output 622, a framing signal 758 is connected to framing signal 693, and a sync reliability signal 788 is connected to sync reliability signal 697. Distance 768 and/or sync reliability signal 788 may be more generically referred to as an example of a sync mark quality metric.

As shown, sync mark detection and framing circuit 791 includes a target filter circuit 796 that applies target filtering to input 706 to yield known preamble pattern 797. A distance calculation circuit 795 calculates a distance ($D_1[k]$) 726 between input 706 and known preamble pattern 797 aligned to input 706 in accordance with the following equation:

$$D_1[k] = \text{Euclidean Distance} = \sum_{k=0}^{19} (\text{Input}[k] - \text{KnownPreamblePattern}[k])^2$$

where k indicates a particular bit pair being compared, and input 706 and known preamble pattern 797 are aligned. Where input 706 is error free, distance ($D_1[k]$) 726 will be zero, and distance ($D_1[k]$) 722 will have a relatively low value where the signal of input 706 is not overwhelmed by the noise. When input 706 transitions from the preamble pattern to the next field (expected to be the sync mark pattern), distance ($D_1[k]$) 726 increases dramatically. Distance ($D_1[k]$) 726 will vary as non-preamble fields are received. Distance (DAD 726 is provided to a summation circuit 728.

In addition, a distance calculation circuit 721 calculates a distance ($D_2[k]$) 724 between input 706 and a known preamble pattern 711 in accordance with the following equation:

$$D_2[k] = \text{Euclidean Distance} = \sum_{k=0}^{19} (\text{Input}[k] - \text{KnownPreamblePattern}[k])^2,$$

where k indicates a particular bit pair being compared, and input 706 and known preamble pattern 711 are aligned. Where input 706 is error free, distance ($D_2[k]$) 724 will be zero, and distance ($D_2[k]$) 724 will have a relatively low value where the signal of input 706 is not overwhelmed by the noise. When input 706 transitions from the preamble pattern to the next field (expected to be the sync mark pattern), distance ($D_2[k]$) 724 increases dramatically. Distance ($D_2[k]$) 724 will vary as non-preamble fields are received. Distance ($D_2[k]$) 724 is provided to summation circuit 728. Summation circuit 728 subtracts distance 726 from distance 724 to yield a differential distance 723. Differential distance 723 is provided to an end of preamble detection circuit 771 that asserts an end of preamble signal 778 when the end of a preamble is identified.

In addition, differential distance 723 is provided to a maximum distance value register circuit 761 that is operable to compare differential distance 723 with a previously stored distance value 768 to determine which is greater, and to retain the greater of the two as distance value 768. The distance value 768 stored in maximum distance value register circuit 761 is set equal to zero when framing signal 758 is asserted indicating that a sync mark was found. Distance value 768 is provided to a maximum distance comparator circuit 781 where it is compared with an expected distance threshold 793. Expected distance threshold 793 may be either fixed or user programmable. Where distance value 768 is greater than expected distance threshold 793, maximum distance comparator circuit 781 asserts sync reliability signal 788 to indicate that a subsequent assertion of framing signal 758 is unreliable. In some cases, differential distance 723 is only accumulated prior to the syncmark pattern. Such accumulation could be a few cycles before the assertion of the syncmark found signal. For example, if the syncmark length is twenty (20), then the accumulation may only accumulate the maximal distance metric five (5) cycles prior to syncmark being found.

In addition, a distance calculation circuit 741 calculates a distance 743 between input 706 and a known sync mark pattern 731 in accordance with the following equation:

$$\text{Distance} = D1 = \sum_{k=0}^{19} (\text{Input}[k] - \text{KnownSyncMarkPattern}[k])^2,$$

where k indicates a particular bit pair being compared. Distance 743 is provided to a sync mark detection circuit 751 that is operable to compare distance 743 with an SM threshold 763. SM threshold 763 may be either fixed or user programmable. Where distance 743 is less than SM threshold value 763, framing signal 758 is asserted to indicate that a sync mark signal has been found.

Turning to FIG. 7, a storage system 900 including a read channel circuit 910 with a sync mark mis-detection avoidance circuitry is shown in accordance with various embodiments of the present invention. Storage system 900 may be, for example, a hard disk drive. Storage system 900 also includes a preamplifier 970, an interface controller 920, a hard disk controller 966, a motor controller 968, a spindle motor 972, a disk platter 978, and a read/write head 976. Interface control-

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ler 920 controls addressing and timing of data to/from disk platter 978. The data on disk platter 978 consists of groups of magnetic signals that may be detected by read/write head assembly 976 when the assembly is properly positioned over disk platter 978. In one embodiment, disk platter 978 includes magnetic signals recorded in accordance with either a longitudinal or a perpendicular recording scheme.

In a typical read operation, read/write head assembly 976 is accurately positioned by motor controller 968 over a desired data track on disk platter 978. Motor controller 968 both positions read/write head assembly 976 in relation to disk platter 978 and drives spindle motor 972 by moving read/write head assembly to the proper data track on disk platter 978 under the direction of hard disk controller 966. Spindle motor 972 spins disk platter 978 at a determined spin rate (RPMs). Once read/write head assembly 978 is positioned adjacent the proper data track, magnetic signals representing data on disk platter 978 are sensed by read/write head assembly 976 as disk platter 978 is rotated by spindle motor 972. The sensed magnetic signals are provided as a continuous, minute analog signal representative of the magnetic data on disk platter 978. This minute analog signal is transferred from read/write head assembly 976 to read channel module 964 via preamplifier 970. Preamplifier 970 is operable to amplify the minute analog signals accessed from disk platter 978. In turn, read channel circuit 910 decodes and digitizes the received analog signal to recreate the information originally written to disk platter 978. This data is provided as read data 903 to a receiving circuit. As part of decoding the received information, read channel circuit 910 performs a sync mark detection process. Such a sync mark detection process may be performed using any detection process known in the art. The sync mark detection is enhanced to avoid mis-detection by assuring that the sync mark is identified within a defined window after the occurrence of a preceding detection. In some embodiments of the present invention, the preceding detection is an end of preamble detection. Read channel circuit 910 may be implemented similar to that discussed above in relation to FIGS. 4a-4b or FIGS. 6a-6b, and the mis-detection avoidance may operate similar to that discussed above in relation to FIGS. 2-3 or FIG. 5.

It should be noted that storage system 900 may be integrated into a larger storage system such as, for example, a RAID (redundant array of inexpensive disks or redundant array of independent disks) based storage system. Such a RAID storage system increases stability and reliability through redundancy, combining multiple disks as a logical unit. Data may be spread across a number of disks included in the RAID storage system according to a variety of algorithms and accessed by an operating system as if it were a single disk. For example, data may be mirrored to multiple disks in the RAID storage system, or may be sliced and distributed across multiple disks in a number of techniques. If a small number of disks in the RAID storage system fail or become unavailable, error correction techniques may be used to recreate the missing data based on the remaining portions of the data from the other disks in the RAID storage system. The disks in the RAID storage system may be, but are not limited to, individual storage systems such as storage system 900, and may be located in close proximity to each other or distributed more widely for increased security. In a write operation, write data is provided to a controller, which stores the write data across the disks, for example by mirroring or by striping the write data. In a read operation, the controller retrieves the data from the disks. The controller then yields the resulting read data as if the RAID storage system were a single disk.

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A data decoder circuit used in relation to read channel circuit 910 may be, but is not limited to, a low density parity check (LDPC) decoder circuit as are known in the art. Such low density parity check technology is applicable to transmission of information over virtually any channel or storage of information on virtually any media. Transmission applications include, but are not limited to, optical fiber, radio frequency channels, wired or wireless local area networks, digital subscriber line technologies, wireless cellular, Ethernet over any medium such as copper or optical fiber, cable channels such as cable television, and Earth-satellite communications. Storage applications include, but are not limited to, hard disk drives, compact disks, digital video disks, magnetic tapes and memory devices such as DRAM, NAND flash, NOR flash, other non-volatile memories and solid state drives.

In addition, it should be noted that storage system 900 may be modified to include solid state memory that is used to store data in addition to the storage offered by disk platter 978. This solid state memory may be used in parallel to disk platter 978 to provide additional storage. In such a case, the solid state memory receives and provides information directly to read channel circuit 910. Alternatively, the solid state memory may be used as a cache where it offers faster access time than that offered by disk platter 978. In such a case, the solid state memory may be disposed between interface controller 920 and read channel circuit 910 where it operates as a pass through to disk platter 978 when requested data is not available in the solid state memory or when the solid state memory does not have sufficient storage to hold a newly written data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of storage systems including both disk platter 978 and a solid state memory.

Turning to FIG. 8, a communication system 800 including a receiver 820 with a ratio metric based sync mark detector circuit is shown in accordance with different embodiments of the present invention. Communication system 800 includes a transmitter 810 that is operable to transmit encoded information via a transfer medium 830 as is known in the art. The encoded data is received from transfer medium 830 by receiver 820. As part of decoding the received data, receiver 820 performs a sync mark detection process. Such a sync mark detection process may be performed using any detection process known in the art. The sync mark detection is enhanced to avoid mis-detection by assuring that the sync mark is identified within a defined window after the occurrence of a preceding detection. In some embodiments of the present invention, the preceding detection is an end of preamble detection. Receiver 820 may be implemented similar to that discussed above in relation to FIGS. 4a-4b, and the mis-detection avoidance may operate similar to that discussed above in relation to FIGS. 2-3 or FIG. 5.

Turning to FIG. 9, a flow diagram 900 shows a method for jitter reduction related to location identification across multiple re-reads of a data set in accordance with some embodiments of the present invention. Following flow diagram 900, a data set is read from a storage medium (block 912). A new distance value for an incremental portion of the read data is then calculated in accordance with the following equation:

$D[k]$ = Euclidean Distance =

$$\sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownPreamblePattern}[k])^2 - \sum_{k=0}^{19} (\text{ReceivedData}[k] - \text{KnownSyncMarkPattern}[k])^2,$$

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where k indicates a particular bit pair being compared, and equalized output 622 and the known preamble pattern are aligned. The known preamble pattern and ideal signal output are the same as those discussed above in relation to FIGS. 6a-6b. A threshold comparison is then applied to determine the occurrence of an end of preamble (block 922). In particular, it is determined whether the following is true:

$$D_{k-1} \leq T < D_k,$$

where T is a threshold calculated as set forth below, D_k is the most recently calculated distance value, and D_{k-1} is the previously calculated distance value. It is determined whether an end of preamble occurred (block 924). Where an end of preamble is not indicated (block 924), the next portion of the data set is selected (block 926) and the processes of blocks 918-924 are repeated for the next portion of the data set.

Alternatively, where an end of preamble is indicated (block 924), it is then determined whether the previous read was the first read of the data set (block 934). Where it is the first read of the data set (block 934), an end of preamble indicator is asserted at a location corresponding to the location of k (i.e., the location where the end of preamble was indicated (block 924)) (block 936), and the values of V_{-2} , V_{-1} , V_0 , V_1 are initialized in accordance with the following equations (block 937):

$$V_{-2} = D_{k-2},$$

$$V_{-1} = D_{k-1},$$

$$V_0 = D_k,$$

and

$$V_1 = D_{k+1},$$

where D_{k-2} is the distance measurement preceding D_{k-1} , and D_{k+1} is the distance measurement corresponding to the data succeeding the data where the end of preamble was identified.

Otherwise, where it is a second or later read of the data set (block 934), a minimum threshold offset (u) is calculated in accordance with the following equation (block 942):

$$u = \operatorname{argmin}_{i \in \{-1, 0, 1\}} \left(\sum_{i=-1}^2 D_{k+m+i} - V_i \right), \text{ for } m \in \{-1, 0, 1\},$$

where the values of $D_{k+m+i} - V_i$ are from the current read. Using this, an end of preamble indicator is asserted at a location corresponding to $k+u$ (i.e., the location at which a threshold cross-over was detected plus the minimum offset) (block 944). By adding this minimum offset, jitter for the location at which the end of preamble indicator is located from one read to the next is mitigated when compared with simply testing the threshold crossover as was done in block 924.

In addition, the values of V_{-2} , V_{-1} , V_0 , V_1 are updated by averaging in the most recent distance measurements (D_{k+u-2} , D_{k+u-1} , D_{k+u} , D_{k+u+1}) in accordance with the following equations (block 935):

$$V_m = [(n-1)/n] * V_m + [1/n] * D_{k+u+m}, \text{ for } 2 \leq n \leq 8 \text{ and } m \in \{-1, 0, 1, 2\};$$

and

$$V_m = 7/8 * V_m + 1/8 * D_{k+u+m}, \text{ for } n > 8 \text{ and } m \in \{-1, 2\}.$$

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The threshold value (T) first mentioned in block 922 above is updated to be the average of V_{-1} and V_0 and a threshold crossing is determined using the same test as described above in relation to block 922, but using the newly calculated threshold (block 938). In particular, it is determined whether the following is true:

$$D_{k-1} \leq T < D_k,$$

where T is the newly calculated average of V_{-1} and V_0 (i.e., $(V_{-1} + V_0)/2$).

It should be noted that the various blocks discussed in the above application may be implemented in integrated circuits along with other functionality. Such integrated circuits may include all of the functions of a given block, system or circuit, or only a subset of the block, system or circuit. Further, elements of the blocks, systems or circuits may be implemented across multiple integrated circuits. Such integrated circuits may be any type of integrated circuit known in the art including, but are not limited to, a monolithic integrated circuit, a flip chip integrated circuit, a multichip module integrated circuit, and/or a mixed signal integrated circuit. It should also be noted that various functions of the blocks, systems or circuits discussed herein may be implemented in either software or firmware. In some such cases, the entire system, block or circuit may be implemented using its software or firmware equivalent. In other cases, the one part of a given system, block or circuit may be implemented in software or firmware, while other parts are implemented in hardware.

In conclusion, the invention provides novel systems, devices, methods and arrangements for data processing. While detailed descriptions of one or more embodiments of the invention have been given above, various alternatives, modifications, and equivalents will be apparent to those skilled in the art without varying from the spirit of the invention. Therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the appended claims.

What is claimed is:

1. A data processing system, the system comprising:

a first pattern identification circuit operable to identify a first pattern in a first subset of a data set;

a second pattern identification circuit operable to identify a second pattern in a second subset of the data set, wherein all of the elements of the second subset are excluded from the first subset;

a distance calculation circuit operable to calculate a distance between the first pattern and the second pattern; and

a quality output circuit operable to provide a quality metric corresponding to the distance between the first pattern and the second pattern.

2. The data processing system of claim 1, wherein the first pattern is an end of preamble pattern and the second pattern is a sync mark pattern, and wherein the system further comprises:

a sync mark found circuit operable to assert a sync mark found signal based upon a combination of the quality metric and identification of the sync mark pattern.

3. The data processing system of claim 1, wherein the first pattern identification circuit includes a differential detection circuit comprising:

a first distance calculation circuit operable to calculate a first distance between a data set and a known sync mark pattern;

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a second distance calculation circuit operable to calculate a second distance between the data set and a predefined pattern;
 a summation circuit operable to combine the first distance with the second distance to yield a combined distance;
 and
 a pattern indicator circuit operable to compare the combined distance with a threshold value and to assert a first pattern indicator corresponding to identification of the first pattern in a data set when the combined distance exceeds the threshold value.

4. The data processing system of claim 3, wherein the combining the first distance and the second distance by the summation circuit includes subtracting the first distance from the second distance to yield the combined distance.

5. The data processing system of claim 1, wherein the first pattern identification circuit includes a multiple sample latching circuit operable to store two or more identified locations of the first pattern in the data set across multiple reads of the data set.

6. The data processing system of claim 5, wherein the multiple sample latching circuit is further operable to select one of the two or more identified locations based upon the two or more identified locations.

7. The data processing system of claim 5, wherein the two or more identified locations are updated through an averaging process.

8. The data processing system of claim 1, wherein the system is implemented as part of an integrated circuit.

9. The data processing system of claim 1, wherein the system is implemented as part of a storage device.

10. A storage device, wherein the storage device comprises:

a storage medium;
 a head assembly disposed in relation to the storage medium and operable to provide a sensed signal corresponding to a data set on the storage medium;
 a read channel circuit including:
 an analog to digital converter circuit operable to sample an analog signal derived from the sensed signal to yield a series of digital samples;
 an equalizer circuit operable to equalize the series of digital samples to yield an equalized output;
 a first pattern identification circuit operable to identify a first pattern in the equalized output, wherein the first pattern is an end of preamble pattern;
 a second pattern identification circuit operable to identify a second pattern in the equalized output, wherein the second pattern is a sync mark pattern;
 a distance calculation circuit operable to calculate a distance between the first pattern and the second pattern; and
 a quality output circuit operable to provide a quality metric corresponding to the distance between the first pattern and the second pattern.

11. The storage device of claim 10, wherein the first pattern is an end of preamble pattern and the second pattern is a sync mark pattern, and wherein the system further comprises:

a sync mark found circuit operable to assert a sync mark found signal based upon a combination of the quality metric and identification of the sync mark pattern.

12. The storage device of claim 10, wherein the first pattern identification circuit includes a differential detection circuit comprising:

a first distance calculation circuit operable to calculate a first distance between a data set and a known sync mark pattern;

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a second distance calculation circuit operable to calculate a second distance between the data set and a predefined pattern;

a summation circuit operable to combine the first distance with the second distance to yield a combined distance;
 and

a pattern indicator circuit operable to compare the combined distance with a threshold value and to assert a first pattern indicator corresponding to identification of the first pattern in a data set when the combined distance exceeds the threshold value.

13. The storage device of claim 12, wherein the combining the first distance and the second distance by the summation circuit includes subtracting the first distance from the second distance to yield the combined distance.

14. A data processing system, the system comprising:

a first pattern identification circuit operable to identify a first pattern in a data set, wherein the first pattern identification circuit includes a multiple sample latching circuit operable to: store two or more identified locations of the first pattern in the data set updated through an averaging process, and select one of the two or more identified locations based upon the two or more locations;

a second pattern identification circuit operable to identify a second pattern in the data set;

a distance calculation circuit operable to calculate a distance between the first pattern and the second pattern;
 and

a quality output circuit operable to provide a quality metric corresponding to the distance between the first pattern and the second pattern.

15. The data processing system of claim 14, wherein the system is implemented as part of an integrated circuit.

16. The data processing system of claim 14, wherein the system is implemented as part of a storage device.

17. The data processing system of claim 14, wherein the first pattern identification circuit includes a differential detection circuit comprising:

a first distance calculation circuit operable to calculate a first distance between a data set and a known sync mark pattern;

a second distance calculation circuit operable to calculate a second distance between the data set and a predefined pattern;

a summation circuit operable to combine the first distance with the second distance to yield a combined distance;
 and

a pattern indicator circuit operable to compare the combined distance with a threshold value and to assert a first pattern indicator corresponding to identification of the first pattern in a data set when the combined distance exceeds the threshold value.

18. The data processing system of claim 17, wherein the combining the first distance and the second distance by the summation circuit includes subtracting the first distance from the second distance to yield the combined distance.

19. The data processing system of claim 14, wherein the first pattern is an end of preamble pattern and the second pattern is a sync mark pattern, and wherein the system further comprises:

a sync mark found circuit operable to assert a sync mark found signal based upon a combination of the quality metric and identification of the sync mark pattern.

20. The data processing system of claim 14, wherein the two or more identified locations of the first pattern in the data set each correspond to different re-reads of the data set.